CLAIMS

1. A DRAM cell comprising

a vertical MOSFET transistor on a substrate having an N doped region forming a buried plate, said vertical transistor being provided with an N+ type doped drain, a P type doped well above said buried plate, and an N+ type doped region forming the transistor source;

a deep trench formed within said substrate, said deep trench having a collar separating said drain from said buried plate, said deep trench having an insolated first region filled with polysilicon and a second region on top of said insulated first region forming said gate, wherein said gate is formed by dual work function materials.

2. The DRAM cell as recited in claim 1 wherein the gate material nearest to said drain has a lower work function than the work function of said second gate material away from said drain.

3. The DRAM cell as recited in claim 1 wherein the gate is capped by a conductive layer formed of either one of said dual work function gate materials.

4. The DRAM cell as recited in claim 3 wherein said conductive layer cap on top of said gate is insulated by spacers.

5. The DRAM cell as recited in claim 1 wherein said ploysilicon region is insulated by an oxide layer.

6. The DRAM cell as recited in claim 1 wherein said upper and lower layer gate materials are selected from the group consisting of W, WSi_2, Al, Cr, Mo, Ti, TiN, polysilicon, $CrSi_2$, $MoSi_2$, $NiSi_2$, Pd_2Si_2, PtSi and $TiSi_2$.

7. A DRAM cell provided with a vertical MOSFET transistor on a substrate having an N doped region forming a buried plate, said vertical transistor being provided with an N+ type doped drain, a P type doped well above said buried plate, and an N+ type doped region forming the transistor source, the DRAM cell comprising:

a deep trench formed within said substrate, said deep trench provided with a collar to separate said drain from said buried plate, said deep trench having an insolated first region filled with polysilicon and a second region on top of said insulated first region forming said gate, wherein said gate is formed by dual work function materials.

8. The method of fabricating a DRAM cell comprising the steps of:

forming a deep trench capacitor within a substrate, said deep trench being partially filled with polysilicon and topped by a trench top oxide;

forming a vertical transistor by diffusing a drain adjoining to the outer surface of said deep trench and contiguous to said trench top oxide;

forming said vertical transistor gate oxide on the walls of said deep trench;

filling the upper portion of said deep trench with a first gate material to a first height of said deep trench, and a second gate material on top of said first gate material, said second gate material only partially filling said deep trench to a second height of said deep trench, said first and second heights being less than the total depth of said deep trench;

forming spacers on the exposed walls of said deep trench;

filling the remainder of said deep trench contacting said uppermost gate material with conductive material, said uppermost gate material being surrounded by said spacers; and

successively implanting into said substrate a buried plate, a well, and said transistor source.

9. The method as recited in claim 8 wherein said first and second gate materials have respectively different work functions.

10. The method as recited in claim 8, wherein N+ in-situ doped polysilicon is deposited at the bottom of said deep trench by chemical-vapor deposition and recessed by reactive ion etch to a predetermined depth that determines the channel length of said vertical transistor.

11. The method as recited in claim 8, wherein said oxide layer deposited around said side-wall of said deep trench above said polysilicon forms a collar oxide, providing vertical isolation between said deep trench and said vertical transistor.

12. The method as recited in claim 11, wherein said gate oxide layer is formed by furnace dry oxidation

13. The method as recited in claim 11 wherein an in-situ doped n+ polysilicon is deposited by chemical vapor deposition and planarized by way of chemical mechanical polishing; said oxide layer acting as a stop layer for said planarization of said polysilicon.

14. The method as recited in claim 8 wherein said uppermost gate material has a higher work function than the lowermost gate material, said uppermost gate material being deposited by chemical vapor deposition.

15. The method as recited in claim 14 wherein the topmost surface is planarized by chemical mechanical polishing, said oxide layer acting as a stop layer for the planarization of said uppermost gate material.